IN THE CLAIMS:

Please amend claims 1, 9, 12, 29 and 31, and add new claims 38-41 as follows:

1. (currently amended) A data transfer system comprising:

a plurality of peripheral interfaces;

a first memory;

a programmable direct memory access module coupling the first memory to each of the plurality of peripheral interfaces, wherein the programmable direct memory access module configures selectively programmable direct memory access data channels between the first memory and, respectively, each one ~~respective ones~~ of the plurality of peripheral interfaces;

a first processor coupled to the programmable direct memory access module and associated with the first memory through a first shared bus, which couples ~~connection coupling~~ both the first processor and the first memory to the programmable direct memory access module;

a second memory coupled to the programmable direct memory access module, wherein the programmable direct memory access module configures the selectively programmable direct memory access data channels between the second memory and, respectively, each one ~~respective ones~~ of the plurality of peripheral interfaces; and

a second processor coupled to the programmable direct memory access module and associated with the second memory through a second shared bus ~~connection, which is~~ independent of the first shared bus ~~connection, coupling~~ which couples both the second processor and the second memory to the programmable memory access module.

2-4. (canceled)

5. (previously presented) The data transfer system of claim 1 wherein the selectively programmable direct memory access data channels are configured between the first memory and the second memory.

6. (previously presented) The data transfer system of claim 1 wherein the programmable direct memory access module includes a programmable processor.

7. (previously presented) The data transfer system of claim 6 wherein the programmable direct memory access module further includes a direct memory access controller coupled to the programmable processor, wherein the programmable processor configures the selectively programmable direct memory access data channels between the first memory and respective ones of the plurality of peripheral interfaces via a dedicated direct memory access data transfer channel of the direct memory access controller.

8. (previously presented) The data transfer system of claim 1 wherein the programmable direct memory access module further comprises a programmable scheduler for prioritizing data transfers over respective ones of the selectively programmable direct memory access data channels.

9. (currently amended) A direct memory access system comprising:

a direct memory access controller establishing a direct memory access data channel and including a first interface for coupling to a first memory;

a second interface for coupling to a plurality of nodes;

a third interface for coupling to a second memory; and

a processor coupled to the direct memory access controller and coupled to the second and third interface, wherein the processor configures the direct memory access data channel to selectively transfer, respectively, data between [[a]] the ~~programmably selectable respective one or more of the~~ plurality of nodes[[,]] and ~~at least one of~~ the first memory, and to selectively transfer, respectively, data between the plurality of nodes and the second memory.

10. (previously presented) The system of claim 9 wherein the plurality of nodes include a plurality of peripheral interfaces.

11. (previously presented) The system of claim 9 further comprising a programmable scheduler coupled to the processor for prioritizing the data transfer via the direct memory access data channel such that the data transfer occurs according to predetermined priorities.

12. (currently amended) A method for performing direct memory access in a direct memory access system including a direct memory access controller having a first interface for coupling to a first memory, a second interface for coupling to a plurality of nodes and a third interface for coupling to a second memory, the method comprising:

receiving a request for a direct memory access data transfer;

configuring code to establish a direct memory access data transfer channel between a node specified by the request via the second interface and at least one of the first memory and the second memory via at least one of the first interface and the third interface of the direct memory access controller, wherein the configuring code is capable of selectively establishing a direct memory access data transfer channel between each of a plurality of nodes and each of the first memory via the first interface and the second memory via the third interface; and

transferring data between the node and the direct memory access controller along the direct memory access data transfer channel.

13. (previously presented) The method of claim 12 wherein the receiving step comprises receiving a timed request for a direct memory access data transfer.

14. (previously presented) The method of claim 12 further comprising prioritizing the data to be transferred via the direct memory access data transfer channel.

15. (previously presented) The method of claim 14 further comprising interrupting the transferring of data in the event a higher priority direct memory access data transfer is required.

16. (previously presented) The method of claim 15 further comprising resuming the interrupted transfer of data upon completion of the higher priority direct memory access data transfer.

17-28. (canceled)

29. (currently amended) A processor communication system, comprising:

a first processor direct memory access interface;

a second processor direct memory access interface;

one or more peripheral ports;

a first data bus for conveying data between said first processor direct memory access interface and said one or more peripheral ports;

a programmable controller comprising a plurality of channel configuration registers in communication with said first data bus for maintaining data communication, with said programmable controller being operable for storing and retrieving data from the plurality of channel configuration registers to establish multiple data transfers between said first processor direct memory access interface and said one or more peripheral ports; and[[;]]

a second data bus coupled to said programmable controller and said second processor direct memory access interface, wherein said programmable controller is operable for establishing multiple data transfers between said second processor direct memory access interface via said second data bus, and at least one of said first processor direct memory interface and said one or more peripheral ports.

30. (canceled)

31. (currently amended) A system as recited in claim 29, wherein said programmable processor prioritizes the multiple data transfers established by storing and retrieving the data from the plurality of channel configuration registers for data transfer between said first processor direct memory access interface, said second processor direct memory access interface, and said one or more peripheral ports.

32. (previously presented) A system as recited in claim 29, wherein said second processor direct memory access interface comprises a digital signal processor direct memory access interface to random access memory associated with a digital signal processor.

33. (previously presented) A system as recited in claim 32, wherein said programmable controller is operable for establishing multiple virtual direct memory access channels between said first processor direct memory access interface, said digital signal processor, direct memory access interface, and said one or more peripheral ports.

34. (previously presented) A system as recited in claim 33, comprising embedded dynamic random access memory for use with the first processor.

35-37. (canceled)

38. (new) A system as recited in claim 29, wherein said plurality of channel configuration registers includes a pointer register.

39. (new) A system as recited in claim 29, wherein said plurality of channel configuration registers includes a channel enable.

40. (new) A system as recited in claim 29, wherein said plurality of channel configuration registers includes a DSP override.

41. (new) A system as recited in claim 29, wherein said plurality of channel configuration registers includes an event override.